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1 Power minimization in IC design: principles and applications

Massoud Pedram
January 1996 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 1 Issue 1
Publisher: ACM Press

Full text available: pdf(550.02 KB) Additional Information: full citation, abstract, references, citings, index terms

Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift in which power dissipation is as important as performance and area. This article presents an in-depth survey of CAD methodologies and techniques for designing low power digital CMOS circuits and systems and describes the many issues facing designers at architectural, logical, and physical levels of design abstraction. It reviews some of the techniques and tool ...

Keywords: CMOS circuits, adiabatic circuits, computer-aided design of VLSI, dynamic power dissipation, energy-delay product, gated clocks, layout, low power layout, low power synthesis, lower-power design, power analysis and estimation, power management, power minimization and management, probabilistic analysis, silicon-on-insulator technology, statistical sampling, switched capacitance, switching activity, symbolic simulation, synthesis, system design

2 Computing curricula 2001

September 2001 **Journal on Educational Resources in Computing (JERIC)**
Publisher: ACM Press
Full text available: pdf(613.63 KB) html(2.78 KB) Additional Information: full citation, references, citings, index terms

3 A design-for-test structure for optimising analogue and mixed signal IC test

A. H. Bratt, A. M. D. Richardson, R. J. A. Harvey, A. P. Dorey
March 1995 **Proceedings of the 1995 European conference on Design and Test EDTC '95**
Publisher: IEEE Computer Society
Full text available: pdf(964.57 KB) Publisher Site Additional Information: full citation, abstract, citings

A new Design-for-Test (DfT) structure based on a configurable operational amplifier, referred to as a "swap amp" is presented that allows access to embedded analogue blocks. The structure has minimal impact on circuit performance and has been evaluated on a custom designed Phase Locked Loop (PLL) structure. A test chip containing faulty and fault free versions of this PLL structure, with and without DfT modifications, has been fabricated and an evaluation of this DfT scheme based on the swap-amp ...

Keywords: DfT modifications, configurable operational amplifier, custom designed phase locked loop, design for testability, design-for-test structure, diagnostics, embedded analogue blocks, integrated circuit testing, mixed analogue-digital integrated circuits, mixed signal IC test, operational amplifiers, phase locked loops, swap amp

4 A new high density and very low cost reprogrammable FPGA architecture

Sinan Kaptanoglu, Greg Bakker, Arun Kundu, Ivan Corneillet, Ben Ting
February 1999 **Proceedings of the 1999 ACM/SIGDA seventh international symposium on Field programmable gate arrays FPGA '99**
Publisher: ACM Press
Full text available: pdf(1.19 MB) Additional Information: full citation, references, citings, index terms

5 Charles W. Bachman interview: September 25-26, 2004; Tucson, Arizona

Thomas Haigh
January 2006 **ACM Oral History interviews**
Publisher: ACM Press
Full text available: pdf(761.66 KB) Additional Information: full citation, abstract

Charles W. Bachman reviews his career. Born during 1924 in Kansas, Bachman attended high school in East Lansing, Michigan before joining the Army Anti Aircraft Artillery Corp, with which he spent two years in the Southwest Pacific Theater, during World War II. After his discharge from the military, Bachman earned a B.Sc. in Mechanical Engineering in 1948, followed immediately by an M.Sc. in the same discipline, from the University of Pennsylvania. On graduation, he went to work for Do ...

6 Special section: Reasoning about structure, behavior and function

B. Chandrasekaran, Rob Milne
July 1985 **ACM SIGART Bulletin**, Issue 93
Publisher: ACM Press
Full text available: pdf(5.13 MB) Additional Information: full citation, abstract, references, citings

The last several years' of work in the area of knowledge-based systems has resulted in a deeper understanding of the potentials of the current generation of ideas, but more importantly, also about their limitations and the need for research both in a broader framework as well as in new directions. The following ideas seem to us to be worthy of note in this connection.

7 The theory of parsing, translation, and compiling

Alfred V. Aho, Jeffrey D. Ullman
January 1972 Book
Publisher: Prentice-Hall, Inc.
Full text available: pdf(98.28 MB) Additional Information: full citation, abstract, references, citings, index terms

From volume 1 Preface (See Front Matter for full Preface)

This book is intended for a one or two semester course in compiling theory at the senior or graduate level. It is a theoretically oriented treatment of a practical subject. Our motivation for making it so is threefold.

(1) In an area as rapidly changing as Computer Science, sound pedagogy demands that courses emphasize ideas, rather than implementation details. It is our hope that the algorithms and concepts presen ...

8 GPGPU: general purpose computation on graphics hardware

David Luebke, Mark Harris, Jens Krüger, Tim Purcell, Naga Govindaraju, Ian Buck, Cliff Woolley, Aaron Lefohn

August 2004 **ACM SIGGRAPH 2004 Course Notes SIGGRAPH '04**

Publisher: ACM Press

Full text available: pdf(63.03 MB) Additional Information: full citation, abstract, citings

The graphics processor (GPU) on today's commodity video cards has evolved into an extremely powerful and flexible processor. The latest graphics architectures provide tremendous memory bandwidth and computational horsepower, with fully programmable vertex and pixel processing units that support vector operations up to full IEEE floating point precision. High level languages have emerged for graphics hardware, making this computational power accessible. Architecturally, GPUs are highly parallel s ...

9 Getting to the bottom of deep submicron II: a global wiring paradigm

Dennis Sylvester, Kurt Keutzer

April 1999 **Proceedings of the 1999 international symposium on Physical design ISPD '99**

Publisher: ACM Press

Full text available: pdf(1.23 MB) Additional Information: full citation, references, citings, index terms

10 Recreational computer graphics: Recreational computer graphics

Andrew Glassner

July 2006 **ACM SIGGRAPH 2006 Courses SIGGRAPH '06**

Publisher: ACM Press

Full text available: pdf(13.82 MB) Additional Information: full citation, abstract

Computer graphics isn't just a bunch of algorithms and programs: it's a gymnasium for the visual imagination, and a tool for investigating the world around us. Graphics can help us understand nature, invent new kinds of patterns and shapes, build up the clarity of our own mind's eye, and experiment with construction tools that would inspire even the most classical sculptors and painters. Going beyond tools and technique, this course invites attendees to think about using computer graphics in new ...

11 Atomic incremental garbage collection and recovery for a large stable heap

Elliot K. Kolodner, William E. Weihl

June 1993 **ACM SIGMOD Record , Proceedings of the 1993 ACM SIGMOD international conference on Management of data SIGMOD '93**, Volume 22 Issue 2

Publisher: ACM Press

Full text available: pdf(1.34 MB) Additional Information: full citation, abstract, references, citings, index terms

A stable heap is storage that is managed automatically using garbage collection, manipulated using atomic transactions, and accessed using a uniform storage model. These features enhance reliability and simplify programming by preventing errors due to explicit deallocation, by masking failures and concurrency using transactions, and by eliminating the distinction between accessing temporary storage and permanent storage.

Stable heap management is useful for programming lang ...

12 Compressionless routing: a framework for adaptive and fault-tolerant routing

J. H. Kim, Z. Liu, A. A. Chien

April 1994 **ACM SIGARCH Computer Architecture News , Proceedings of the 21ST annual international symposium on Computer architecture ISCA '94**, Volume 22 Issue 2

Publisher: IEEE Computer Society Press, ACM Press

Full text available: pdf(1.17 MB) Additional Information: full citation, abstract, references, citings, index terms

Compressionless Routing (GR) is a new adaptive routing framework which provides a unified framework for efficient deadlock-free adaptive routing and fault-tolerance. CR exploits the tight-coupling between wormhole routers for flow control to detect potential deadlock situations and recover from them. Fault-tolerant Compressionless Routing (FCR) extends Compressionless Routing to support end-to-end fault-tolerant delivery. Detailed routing algorithms, implementation complexity and performance sim ...

13 A survey of research and practices of Network-on-chip

Tobias Bjerregaard, Shankar Mahadevan

June 2006 **ACM Computing Surveys (CSUR)**, Volume 38 Issue 1

Publisher: ACM Press

Full text available: pdf(1.41 MB) Additional Information: full citation, abstract, references, index terms

The scaling of microchip technologies has enabled large scale systems-on-chip (SoC). Network-on-chip (NoC) research addresses global communication in SoC, involving (i) a move from computation-centric to communication-centric design and (ii) the implementation of scalable communication structures. This survey presents a perspective on existing NoC research. We define the following abstractions: system, network adapter, network, and link to explain and structure the fundamental concepts. First, r ...

Keywords: Chip-area networks, GALS, GSI design, NoC, OCP, SoC, ULSI design, communication abstractions, communication-centric design, interconnects, network-on-chip, on-chip communication, sockets, system-on-chip

14 Dynamic Standby Prediction for Leakage Tolerant Microprocessor Functional Units

Ahmed Youssef, Mohab Anis, Mohamed Elmasry

December 2006 **Proceedings of the 39th Annual IEEE/ACM International Symposium on Microarchitecture MICRO 39**

Publisher: IEEE Computer Society

Full text available: pdf(192.47 KB) Additional Information: full citation, abstract, index terms

Leakage power is projected to comprise approximately 50% of the processor's power for sub 65nm technologies. Much of this power is consumed in the processor's functional units. Accordingly, leakage control techniques are employed to reduce leakage in these functional units. Many of these techniques are dynamic and are based on an input sleep signal to initiate a low leakage mode. However, since most of these leakage control techniques are based on circuit level schemes, such techniques inherentl ...

15 Estimation Needs for Future Networking Systems Interconnect: Estimation needs for future networking systems interconnect

Sudhakar Muddu

April 2002 **Proceedings of the 2002 international workshop on System-level interconnect prediction SLIP '02**

Publisher: ACM Press

Full text available: Additional Information:

pdf(150.16 KB) full citation, abstract, index terms

Architectures for new products in the networking systems space will make tradeoffs in many dimensions, including density, cost, performance (functionality, throughput, latency, etc.) and power. This paper describes metrics for system-level interconnects in networking applications, along with associated estimation requirements.

16 A floorplan-based planning methodology for power and clock distribution in ASICs

Joon-Seo Yim, Seong-Ok Bae, Chong-Min Kyung

June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation DAC '99**

Publisher: ACM Press

Full text available: pdf(1.19 MB) Additional Information: full citation, references, citings, index terms

17 Signal processing at 250 MHz using high-performance FPGA's

Brian Von Herzen

February 1997 **Proceedings of the 1997 ACM fifth international symposium on Field-programmable gate arrays FPGA '97**

Publisher: ACM Press

Full text available: pdf(1.06 MB) Additional Information: full citation, references, citings, index terms

18 Interconnect noise avoidance methodologies & slew rate prediction: Interconnect and noise immunity design for the Pentium 4 processor

Rajesh Kumar

June 2003 **Proceedings of the 40th conference on Design automation DAC '03**

Publisher: ACM Press

Full text available: pdf(407.27 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes the key challenges, design methods, CAD and learnings in the area of interconnect and noise immunity design for the Intel Pentium 4 processor.This high frequency (currently at 3 Ghz with 6 Ghz execution core) design required aggressive domino, pulsed and other novel high speed circuit families that are very noise sensitive. Controlling interconnect delay, capacitive and inductive coupling is of paramount importance at such high frequencies and edge rates, made more difficult ...

19 Performance measurement/content inspection: Design and analysis of an NoC architecture from performance, reliability and energy perspective

Jongman Kim, Dongkook Park, Chrysostomos Nicopoulos, N. Vijaykrishnan, Chita R. Das

October 2005 **Proceedings of the 2005 symposium on Architecture for networking and communications systems ANCS '05**

Publisher: ACM Press

Full text available: pdf(867.80 KB) Additional Information: full citation, abstract, references, index terms

Network-on-Chip (NoC) architectures employing packet-based communication are being increasingly adopted in System-on-Chip (SoC) designs. In addition to providing high performance, the fault tolerance and reliability of these networks is becoming a critical issue due to several artifacts of deep sub-micron technologies. Consequently, it is important for a designer to have access to fast methods for evaluating the performance, reliability, and energy-efficiency of an on-chip network. Towards this ...

Keywords: adaptive routing, networks-on-chip, reliability

20 Soviet Computer Technology--1959

March 1960 **Communications of the ACM**, Volume 3 Issue 3

Publisher: ACM Press

Full text available: pdf(8.23 MB) Additional Information: full citation, citings

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L2	66	(341/58).CCLS.	US-PGPUB	AND	ON	2007/06/06 10:10
L3	12	signal buffer track DC flip	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2007/06/06 10:10
L4	0	signal buffer track DC flip and l1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2007/06/06 10:10

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L7	0	signal track DC flip and l2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2007/06/06 10:11
L8	0	signal track DC flip and l2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2007/06/06 10:11

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L11	26	DC flip and l1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2007/06/06 10:12
L12	1	DC flip and l2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2007/06/06 10:25

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L14	0	bias transistor base dc and l1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2007/06/06 10:25